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DESIGN AVOLTAGE REFERENCE CIRCUIT WITHOUT USING BIPOLAR TRANSISTORS

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ABSTRACT

In this paper, a voltage reference circuit using MOSFET transistors based on difference between the gate voltage - source a transistor of PMOS and the NMOS transistor type was introduced. To reduce the flow, passive circuit elements is minimized and all transistors are biased in the sub-threshold. Changes proposed in circuit output voltage were too low and by changing the supply voltage as much as 900 mV, the output voltage had only 90 mV change. Also, by changing the temperature from 40 to 120 degrees only 5 mV changes happened. In other words, the temperature changes were from 37 ppm / ° c. In this design, only the MOSFET transistor was used and bipolar transistors were not used. Supply voltage was 1.8 V and output voltage was 850 mV.

Keywords: Voltage reference circuit, sub threshold region, temperature changes, low power consumption

INTRODUCTION

An important part in analog integrated circuits design is to design and manufacture of voltage reference flows with well-defined values. Because it is integrated on the chip, usually used in reference circuits called band gap voltage reference circuits [1-5]. The circuit design of the reference makes the voltage independent of temperature possible. A common use of the reference voltage is for the analog-to-digital voltage change in which the input voltage is compared with several levels to determine the corresponding digital value**.** In fact, a reference voltage source circuit should be able to use an external power supply voltage to a lower voltage levels produce. For example, in0.18 um CMOS technology, the supply voltageis1.8 V but in the design of integrated circuits for the biasing the circuitry and transistors of different parts of the various

voltages are required. The task of the reference voltage circuits is to produce different voltage levels. The voltage produced by the circuit should be fixed and should not change by changes in temperature, processing or voltage. In practice the reference voltage with these changes which are called PVT change is said to be minimal. [6-9]. Voltage reference circuit has various types which can be divided into four general categories. These categories in general describe the technology in which reference voltage is made and the way in which the output voltage is produced. In the MOSFET technologies, the most obvious way to make the threshold voltage is the voltage reference. In bipolar technology, the bisymmetric link of the bipolar transistor can be used to deliver the band gap silicon voltage to be used as a reference voltage. In addition, bipolar transistors can be manufactured in MOSFET technology which is sufficient to extract the silicon band gap voltage. The other MOSFET circuit can be used to generate the reference voltage.

MOSFET transistors and power consumption is much lower, especially because of the benefits it has compared to bipolar transistors. It is desirable that the reference voltage circuits are designed with MOSFET transistors. One of the production methods for CMOS reference is using different threshold voltage difference between the two to produce a stable reference voltage. If there is a technology with two different threshold voltage for equal to cut, the voltage can be reduced from one another and the output voltage is independent of temperature. If parts are of the same type, it is assumed that the temperature dependence of the same but have different threshold voltages. A linear regulator that is without self has no ripple and low noise converters are widely used in many devices that use batteries. Linear Regulators were made by BJT technology in the past.

However, power efficiency is low for low power operation because the flow is dependent on the load current and large voltage fluctuations. With the rapid evolution of technology CMOS, many linear regulators are available with low variation (LDO).

The earth is independent of the LDO and can operate at very low voltages which are suitable for single-cell and two cell applications. A reference voltage required for LDO design and a reference voltage with very low dependence on temperature and power supply produces to determine the output voltage LDO.As mentioned above, the reference voltage is usually a band gap reference which can be used in any standard CMOS technology using BJT. As an option, the reference voltage in MOS technology can be based on the difference in threshold voltage and ion-selective planting and is made by the differences between work function and the gate gross margin rate. But these solutions

make the construction process complicated and are not proper for standard CMOS technologies with low prices [10, 11].In addition, in deep submicron CMOS technologies, the hallmarks of BJT became worse [10]. In this paper, as a solution to this challenge, MOSFET transistors are biased in the area below the threshold. In the case of very low flow circuit drawn power consumption is very low. Accordingly, a band gap reference voltage using MOSFET transistors will be designed without using BJT transistors. In fact, in this article BJT transistors is used instead of MOSFET transistors and a stable voltage converter circuit is designed with low power consumption.The circuit is designed for 40-to 120 ° C temperature range and various Corners tt, ss, ff, with very little will change. Voltage reference circuits, often in Figure1 is a quantity with positive changes with respect to temperature (PTAT) and quantity and another one is combined with negative changes with respect to temperature (CTAT), low temperature to voltage or current occur with respect to temperature changes. In terms of performance, voltage reference circuits can be divided into five categories [11-15]:

1. The total voltage of PTAT and CTAT
2. Sum of a CTAT voltage and a PTAT current multiplied by resistance R
3. Sum of a CTAT current multiplied by resistance R and a PTAT voltage
4. Total current CTAT and PTAT, multiplied by the resistance R
5. The dispute committee or PTATCTAT

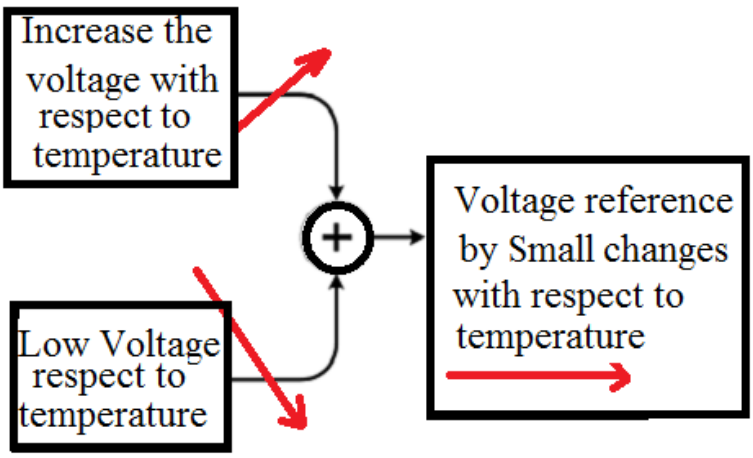

Figure 1: Shows the performance of the voltage reference circuit

Thereferencevoltageof1 VREF is created by the sum VCTAT with a coefficient α and VPTAT βas a factor. Since both terms are voltage, a reference voltage is called Type 1

mode voltage. It should be noted that positive TC is obtained from the voltage difference between the two bipolar transistors which operate at two different flow or the difference between the gate –source voltage in MOS transistors under the sub-threshold bias and negative TC is directly obtained by the voltage of a bipolar transistor, voltage connected to pn junction diode or VGS of a transistor voltage MOS.

The proposed voltage reference circuit

In many applications that can be received wireless and limited, current consumption is very important. Reference work based on the difference between VGS transistors usually use two resistors to create a voltage difference and the same temperature throughout the period of use which increases the current consumption. The first step towards removing this resistance is to reduce the current consumption. Therefore, as shown in Figure 2, the resistors are removed in order to compensate for the elimination of resistance and the creation of value for the gate-source voltage of NMOS transistors, , a third transistor is added. As a result, the output voltage will be as follows:

$$V_{REF} = V_{GS2} + V_{GS3} - V_{GS1} \qquad (1)$$

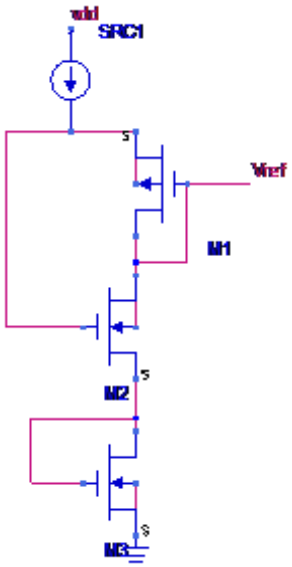

Figure 2: a simplified plan view of the proposed circuit voltage reference

The next step is to design in the sub-threshold. This could further reduce current consumption in the lead. All the proposed circuit voltage reference is shown in Figure 3. This includes core reference voltage, and the biased circuit. In fact the whole project has used the transistor instead of the current source.

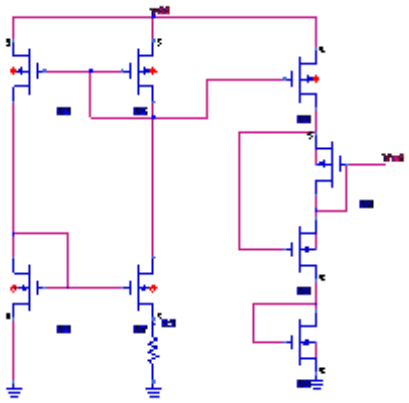

Figure 3: Shows the proposed voltage reference

As mentioned above, the bias circuit in the region is below the threshold. MOSFET transistor current-voltage relationship in this area is as follows:

$$I_D = \mu_n C_{ox} \frac{W}{L} V_T^2 \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \quad (2)$$

Where n is the sub-threshold slope, and VT is the thermal voltage which is rewritten in the equation:

$$V_{GS} = nV_T Ln \frac{I_D}{\mu_n C_{ox} \frac{W}{L} V_T^2} + V_{th} \quad (3)$$

As a result, bias current is equal to:

$$I_D = \frac{1}{R_1}(V_{GS8} - V_{GS7}) =$$

$$\frac{nV_T}{R_1}\left[Ln\frac{(W/L)_7}{(W/L)_8}\right] = \frac{nkT_0}{qR_1}\left[Ln\frac{(W/L)_7}{(W/L)_8}\right]\frac{T}{T_0} = I(T_0)\frac{T}{T_0} \quad (4)$$

Where I (T¬0) sentence is independent of temperature andT0isroom temperature. The temperature dependence of PMOS and NMO S transistors Vth can be written as[14]:

$$V_{thp}(T) = V_{thp}(T_0) - \beta_{thp}(T - T_0) \quad (5)$$

$$V_{thn}(T) = V_{thn}(T_0) - \beta_{thn}(T - T_0) \quad (6)$$

In which are temperature constants thnβ and thpβ on the NMOS and PMOS threshold voltages. The temperature dependence of PMOS and NMOS transistors, respectively is written as follows [14]:

$$\mu_p(T) = \mu_p(T_0)\left(\frac{T}{T_0}\right)^{-\beta_{\mu p}} \quad (7)$$

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-\beta_{\mu n}} \quad (8)$$

For the technology, thp = 0.355βp = 0.13, μβn = 1.024, μβ0.18 um, and thn = 0.255β, respectively. Given the above relationships to determine the temperature dependence of the proposed reference voltage, the equation (1) is used to take the derivative of temperature:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{GS2}}{\partial T} + \frac{\partial V_{GS3}}{\partial T} - \frac{\partial V_{GS1}}{\partial T} \quad (9)$$

$$= \frac{nk}{q} Ln\left[\frac{\mu_p(T_0)(T_0)^{\beta_{\mu p}-1}\left(\frac{W}{L}\right)_1 MI(T_0)}{(\mu_n(T_0))^2 (T_0)^{2\beta_{\mu n}}\left(\frac{W}{L}\right)_2\left(\frac{W}{L}\right)_3 C_{ox}\left(\frac{k}{q}\right)^2}\right] +$$

$$\frac{nk}{q} Ln\left(T^{\beta_{\mu n}-1}\frac{T^{\beta_{\mu n}-1}}{T^{\beta_{\mu p}-1}}\right) + \frac{nk}{q}\left(2\beta_{\mu_n} - \beta_{\mu_p} - 1\right) + \beta_{thp} - 2\beta_{thn}$$

By equaling the result of the equation (9) as zero, can be provided below for reference ratio core in voltage transistors to remove the temperature dependence of the reference voltage.

$$Ln\left[\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2\left(\frac{W}{L}\right)_3}\right] =$$

$$-Ln\left[\frac{MI(T_0)T^{2\beta_{\mu n}-\beta_{\mu p}-1}}{(T_0)^{2\beta_{\mu n}} C_{ox}\left(\frac{k}{q}\right)^2}\right] - Ln\left[\frac{\mu_p(T_0)(T_0)^{\beta_{\mu p}-1}}{(\mu_n(T_0))^2}\right] +$$

$$\beta_{\mu p} - 2\beta_{\mu n} + 1 + \frac{q}{nk}\left(-\beta_{thp} + 2\beta_{thn}\right) \quad (10)$$

Figure 4 shows the output voltage reference circuit with temperature changes. It can be seen that the circuit temperature changefrom-40to 120degreesisonly5 Mv changes. In other words, the temperature changesfrom37 ppm / ° c.

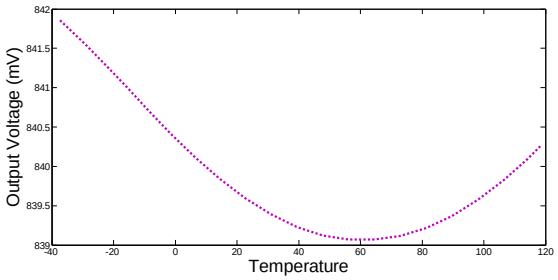

Figure 4: Proposed changes output voltage reference circuit with temperature

Figure 5 shows the output voltage to the supply voltage. We can see that the supply voltage change as much as900 mV, output voltage is changed only90 mV.

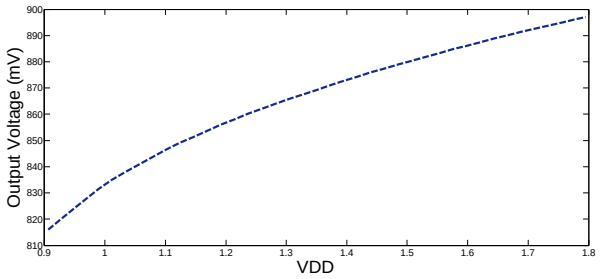

Figure 5: Shows the output voltage changes with supply voltage

In Figure 6 reference voltage noise density is shown. Due to the density obtained at the frequency of 100 Hz noise of Hz√15 nV.

Figure 7showsa diagram of the proposed PSRR for reference. We can see thatthePSRRat100 Hz frequency is equal to-90 dB.

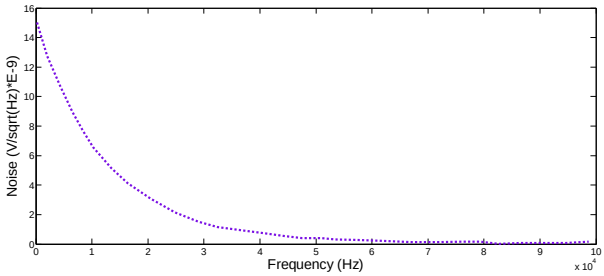

Figure 6: The proposed reference voltage noise density

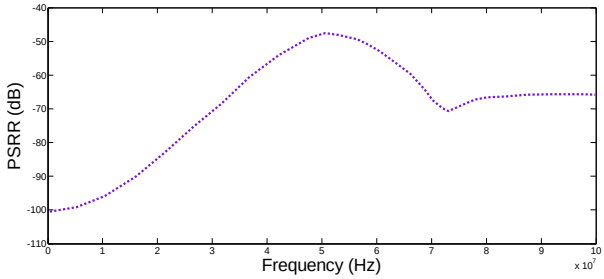

Figure 7: The proposed PSRR voltage reference

The proposed voltage reference circuit along with recent works is presented in Table1. The proposed plan is in a wider temperature range and current consumption and acceptable TC. In order tousesmart cards and PSRR, this circuit is much better than other authorities.

CONCLUSION

In this paper, a reference voltage CMOS and withoutbipolartransistorsusing0.18 μm CMOS technology was designed and proposed .The voltage reference was biased in sub-threshold area and so power consumption is very low. The proposed circuit temperature changes and PSRR is better than previous work.

Table 1: the proposed voltage reference and comparison with previous work

	[14]	[15]	[16]	[17]	[6]	This article
technology (μmCMOS)	0.6	0.35	0.35	0.18	0.35	0.18
Temperature range (centigrade)	0-100	-20-80	-40-80	0-100	-25-83	-40-120
Feed voltage(V)	1.4-3	1.4-3	1-4	1.2-2	1.5-3.3	0.9-1.8
Reference voltage(V)	0.309	0.745	0.19	0.356	1.038	1.275
Temperature constant(ppm/°C)	36.9	7	16.9	3.58	87	37
PSRR (dB)	-47	-45	-41	-100	-49	-92

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